

In the Claims

The following is a marked-up version of the specification with the language that is underlined (“___”) being added and the language that contains strikethrough (“—”) being deleted:

1. (Currently amended) A low capacitance depletion mode SCR and NFET element integrated circuit semiconductor device structure with associated parasitic bipolar transistors on a substrate for the purpose of providing electrostatic voltage discharge protection to the active semiconductor devices, comprising:

A first doped region of opposite ~~dopant~~dopant than said substrate;

a second doped region, of opposite dopant than said first doped region, within said first doped region ~~of opposite dopant than said second doped region~~;

a plurality of third doped regions within said substrate of opposite ~~dopant~~dopant than said substrate;

a gate ~~structure~~ element overlaying said substrate surface between a first element and second element of said third doped regions;

a gate ~~structure~~ element overlaying said substrate surface between a third element and fourth element of said third doped regions;

a first isolation element between said second element of said third doped region and a first side of said second doped region;

a second isolation element between said third element of said third doped region and a second side of said second doped region;

a plurality of fourth doped regions within said substrate of similar ~~doped~~dopant as said substrate;

an electrical ~~connection~~conductor system for said second doped region;

an electrical ~~connection~~conductor system for said first and fourth elements of said third doped regions and for the first and second elements of said fourth doped regions;
and

a surface passivation layer for said ESD protection device.

2. (Original) The structure according to claim 1 wherein said substrate consists of silicon semiconductor material doped to a concentration between $1\text{E}15$ and $1\text{E}16 \text{ a/cm}^3$.

3. (Original) The structure according to claim 1 wherein said first doped region is doped with a donor element such as As to a concentration between $5\text{E}15$ to $1\text{E}18 \text{ a/cm}^3$ and has a width between 0.5 to $6 \mu\text{m}$ and a depth between 0.5 to $6 \mu\text{m}$ to form a N-well.

4. (Currently amended) The structure according to claim 1 wherein said second doped region is doped with an acceptor element such as boron to a concentration between $1\text{E}19$ and $1\text{E}21 \text{ a/cm}^3$ to form a ~~N-well~~ P+ contact region.

5. (Currently amended) The structure according to claim 1 wherein said plurality of third doped regions are doped with an ~~acceptor~~ donor element such as arsenic to a concentration of between $1\text{E}19$ and $1\text{E}21 \text{ a/cm}^3$.

6. (Currently amended) The structure according to claim 1 wherein said first and fourth elements of the said third doped regions form the N+ ~~drain~~source regions of NFET elements.

7. (Original) The structure according to claim 1 wherein said second and third elements of the said third doped regions form the drain regions of NFET elements and are electrically floating.

8. (Original) The structure according to claim 1 wherein said gate elements are comprised of gate oxide to a thickness between 50 and 300Å and polysilicon to a thickness between 3000 and 6000Å.

9. (Currently amended) The structure according to claim 1 wherein said polysilicon is doped with a donor element to a concentration between 1×10^{19} and 1×10^{21} a/cm³.

10. (Original) The structure according to claim 1 wherein said isolation elements consist of shallow trench isolation structures with a width of between 0.1 and 3 μm and a depth of between 0.5 and 4μm.

11. (Original) The structure according to claim 1 wherein said isolation elements are filled with a first layer of SiO₂ to a thickness of between 50 and 500 Å and then filled with a second layer of SiO₂ to said substrate surface.

12. (Currently amended) The structure according to claim 1 wherein said plurality of fourth doped regions are doped with an acceptor element such as boron to a concentration of between $1\text{E}19$ and $1\text{E}21 \text{ a/cm}^3$ to form P+ contact ~~elements~~ regions for said substrate.

13. (Currently amended) The structure according to claim 1 wherein said electrical ~~connection~~conductor system for said second doped region consists of aluminum metallurgy or aluminum doped with 1% silicon metallurgy, and is connected to a first voltage source consisting of the input pad of said active semiconductor devices.

14. (Currently amended) The structure according to claim 1 wherein said electrical ~~connection~~conductor system for said first and fourth elements of said third doped regions consists of aluminum metallurgy or aluminum doped with 1% silicon metallurgy, and is connected to a first voltage source consisting of the input pad of said active semiconductor devices.

15. (Original) The structure according to claim 1 wherein said surface passivation layer for said ESD protection device consists of deposited SiO_2 doped with boron and phosphorous to form BPSG.